Mount Kenya University

UNIVERSITY EXAMINATION 2014/2015

SCHOOL OF PURE AND APPLIED SCIENCES
DEPARTMENT OF ENGINEERING

BACHELOR OF SCIENCE LABORATORY TECHNOLOGY
SCHOOL BASED

UNIT CODE: BEG2112 **UNIT TITLE: BASIC DIGITAL ELECTRONICS AND LOGICS**

DATE: APRIL/MAY 2015 **MAIN EXAM** **TIME: 2 HOURS**

Instructions: Answer Question ONE and ANY other TWO

QUESTION ONE (30 MARKS)

Question one

(a) Distinguish between a digital quantity and an analogue quantity (2mks)

(b) State one advantage and one disadvantage of synchronous counters over asynchronous counters (2mks)

(c) Distinguish between sequential logic and combinational logic (2mks)

(d) An 8-bit digital to analogue converter (DAC) produces V_{out} of 0.05V for digital input 00000001. Determine both its full scale output and resolution. (2mks)

(e) Define the following as applied to digital logic families (i) V_{OH}(min) (ii) V_{IH}(min) (2mks)

(f) Convert $X = (\overline{A} + \overline{B})(A + B + C)$ to standard form. (2mks)

(g) Draw a logic symbol of a 2-input AND gate and give its truth table. Give a diode circuit implementation of AND gate and sketch output waveform for the input waveforms A and B (4mks)

(h) Draw a circuit diagram to show how AND gate can be implemented using NOR gates only. (3mks)

(i) Define the following terms used in combinational logic design: literal, minterm and maxterm. (3mks)

(j) Explain why CMOS inputs should never be left unconnected (floating)? (3mks)

(k) Briefly describe how a decoder works. (3mks)

(l) Define fan-out and fan-in as applied to digital circuits. (2mks)

QUESTION TWO (20 MARKS)

(a) (i) Convert decimal number 93.347 to binary. (ii) Hexadecimal number $F3_{16}$ to decimal (iii) Octal number 7765_8 to decimal. (3mks)

(b) Perform the following binary arithmetic (i) $1101_2 + 1011_2$ (ii) 00110100_2-00001010_2 (iii) $1001_2 \times 110_2$ (iv) $1100_2 \times 011_2$ (4mks)

(c) Write down the truth table for a three input NAND gate. (3mks)

(d) Use Boolean Algebra to show that $(\overline{A}.\overline{C}) + A.\overline{C} + B.C = B + \overline{C}$ (4mks)

(e) Sketch the structures of both totem-pole and open collector outputs for TTL devices. (6mks)

QUESTION THREE (20 MARKS)

(a) Design a logic circuit having three inputs (A, B, C) that will have its output high only when a majority of the input are high. (5mks)

(b) In digital systems, shift registers are very important components. Draw a block diagram to show how four d-type flip-flops can be converted to form serial in/serial out shift register. (4mks)

(c) Define fan-out and fan-in as applied to digital circuits. (2mks)

(d) A74S00 NAND gate has the specified currents: I_{OH}=-1mA, I_{IH}=50μA, I_{QL}=20mA, I_{IL}=-2mA. Determine the values of fan-out and fan-in for this gate. (3mks)

(e) By making appropriate substitutions for gates, draw circuits that are equivalent to the one given in figure 5 below using (a) OR gates and invertors only (b) NAND gates and invertors only (6mks)

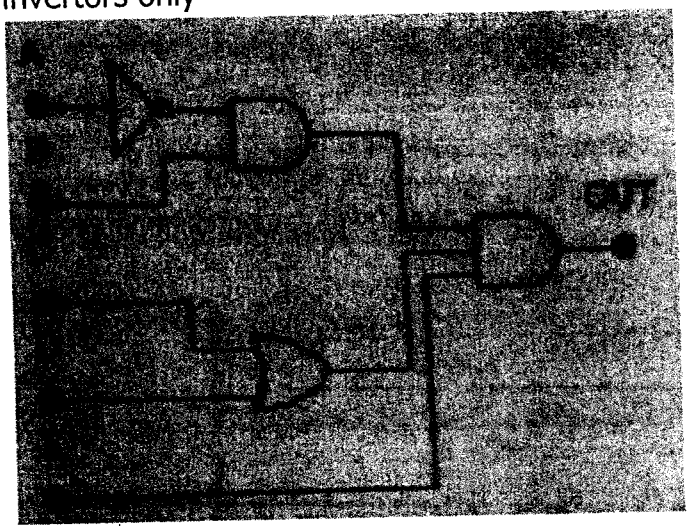

Figure 5.

NAND gates and Invertors

QUESTION FOUR (20 MARKS)

(a) Give a logic symbol of SR flip-flop. Explain briefly how it works and derive its truth table. (6mks)

(b) What is the difference between NOR and the NAND implementation in (4a) above. (2mks)

(c) Use both Boolean algebra and Karnaugh Maps to reduce the following equations to a circuit with the fewest number of gates. (6mks)

(d) Draw up the truth table for the half-adder and show that $\Sigma = A \oplus B$ and $C_{out} = A.B$ (3mks)

(e) Show how two half-adders can be interconnected to implement a full-adder. (3mks)

QUESTION FIVE (20 MARKS)

(a) (i) Sketch the structures of both totem-pole and open collector outputs for TTL devices. (6mks)

(ii) Briefly explain advantages of a tri-state output stage in (5b) above. (2mks)

(b) Give a block diagram of a half-adder (2mks)

(c) Write the un-simplified minterm Boolean expression for the truth table below and then draw a 4-variable Karnaugh Map. Plot six 1s on the map from the Boolean expression developed. Draw the appropriate loops around groups of 1s on the map. (10mks)

Inputs				Output	Inputs				Output
A	B	C	D	Y	A	B	C	D	Y
0	0	0	0	1	1	0	0	0	0
0	0	0	1	0	1	0	0	1	0
0	0	1	0	0	1	0	1	0	1
0	0	1	1	0	1	0	1	1	1
0	1	0	0	1	1	1	0	0	0
0	1	0	1	0	1	1	0	1	0
0	1	1	0	0	1	1	1	0	1
0	1	1	1	0	1	1	1	1	1

$$\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot \overline{C} \cdot \overline{D} + A \cdot \overline{B} \cdot C \cdot \overline{D} + A \cdot \overline{B} \cdot C \cdot D + A \cdot B \cdot C \cdot \overline{D} + A \cdot B \cdot C \cdot D = Y$$

$Y = BC + A + ABC + AB.$